CLAIMS

What is claimed is:

1. A method of forming a diffusion barrier for a semiconductor device, comprising:

providing a semiconductor substrate; and

forming a substantially amorphous diffusion barrier layer overlying at least a portion of the semiconductor substrate, where the barrier layer comprises a multilayer diffusion barrier comprised of a plurality of sub-layers, each having a thickness predetermined to result in a substantially amorphous state, to inhibit diffusion of a chemical species through the diffusion barrier.

2. A method as in claim 1, wherein the sub-layers are comprised of alternating layers of at least two different materials.

3. A method as in claim 2, where one of the materials is scandium (Sc).

4. A method as in claim 2, where one of the materials is copper (Cu).

5. A method as in /claim 2, where one of the materials is yttrium (Y).

6. A method as in claim 2, where one of the materials is lanthanum (La).

7. A method as in claim 2, where one of the materials is tantalum (Ta).

8. A method as in claim 2, where one of the materials is a metal nitride.

9. A method as in claim 2, where one of the materials is an oxide.

10. A method as in claim 2, wherein the at least two materials selected to comprise the sub-layers are substantially immiscible.

11. A method as in .claim 2, wherein the at least two materials selected to comprise the sub-layers exhibit mutual adhesion.

12. A method as in claim 1, where the sub-layers each have a thickness in the range of about two to about fifteen atoms.

13. A method as in claim 1, where the sub-layers each have a thickness in the range of about two to about ten atoms.

14. A method as in claim 1, where the sub-layers each have a thickness in the range of about two to about five atoms.

15. A method as in claim 1, wherein forming the diffusion barrier layer comprises a physical vapor deposition (PVD) process.

16. A method as in claim 1, wherein forming the diffusion barrier layer comprises an atomic layer deposition (ALD) process.

17. A method as in claim 1, wherein forming the diffusion barrier layer comprises a chemical vapor deposition (CVD) process.

18. A method as in claim 1, wherein forming the barrier layer overlying the semiconductor substrate forms at least three sub-layers.

19. A diffusion barrier comprising a plurality of stacked sub-layers, each sub-layer having a thickness predetermined to inhibit the formation of a crystalline lattice, to inhibit diffusion of a chemical species through the diffusion barrier.

20. A diffusion barrier as in claim 19, wherein the sub-layers are comprised of alternating

layers of at least two different materials.

21. A diffusion barrier as in claim 20, where one of the materials is scandium (Sc).

22. A diffusion barrier as in claim 20, where one of the materials is copper (Cu).

23. A diffusion barrier as in claim 20, where one of the materials is yttrium (Y).

24. A diffusion barrier as in claim 20, where one of the materials is lanthanum (La)

25. A diffusion barrier as in claim 20, where one of the materials is tantalum (Ta).

26. A diffusion barrier as in claim 20, where one of the materials is a metal nitride.

27. A diffusion barrier as in claim 20, where one of the materials is an oxide.

28. A diffusion barrier as in claim 20, wherein the at least two materials selected to comprise the sub-layers are substantially immiscible.

29. A diffusion barrier as in claim 20, wherein the at least two materials selected to comprise the sub-layers exhibit mutual adhesion.

30. An integrated circuit comprising a substrate, having an electrically conductive feature disposed on said substrate, further comprising a diffusion barrier interposed between said substrate and said electrically conductive feature, said diffusion barrier comprising a plurality of stacked sub-layers, each sub-layer having a thickness predetermined to inhibit the formation of a crystalline lattice.

31. An integrated circuit as in claim 30, where at least one of said sub-layers is comprised of a metal.

32. A circuit structure comprising a substrate and an electrical interconnect comprised of copper (Cu), further comprising a diffusion barrier interposed between said substrate and said electrical interconnect, said diffusion barrier comprising a plurality of stacked sub-layers.

33. A circuit structure as in claim 32, where said sub-layers are comprised of copper (Cu) and tantalum (Ta).

34. A circuit structure as in claim 32, where said sub-layers are comprised of scandium (Sc) and tantalum (Ta).

35. A circuit structure as in claim 32, where said sub-layers are comprised of yttrium (Y) and tantalum (Ta).

36. A circuit structure as in claim 32, where said sub-layers are comprised of lanthanum (La) and tantalum (Ta).

37. A circuit structure as in claim 32, where at least one of the sub-layers is comprised of a metal nitride.

38. A multilayer diffusion barrier comprised of atomically thin films in which the surface adhesion of each interface inhibits the formation of a lattice in the bulk of the individual film layers, inhibiting diffusion across the barrier.

39. A multilayer diffusion barrier as in claim 38, where the films thickness is in a range of about two atoms to about five atoms.

40. A multilayer diffusion barrier as in claim 38, where the films thickness is in a range of about 0.4 nanometers to about 1.5 nanometers.

41. A multilayer structure comprised of three or more sub-layers, wherein the interface of each of the sub-layers dominates the lattice formation on the sub-layers, preventing the

formation of a lattice and grain boundaries, to inhibit diffusion of a chemical species through the barrier.

42. A multilayer structure as in claim 41, where each of the sub-layers is comprised of a metal.

43. A multilayer diffusion barrier for inhibiting diffusion of chemical species there through, comprising a plurality of stacked layers comprised of alternating films of at least two different metals, the thickness of each of said films being predetermined to substantially eliminate work hardening.